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חוק הפטנטים, תשכ"ז – 1967
PATENTS LAW, 5727-1967

בקשה לפטנט
Application For Patent

לשימוש הלשכה
For Office Use

מספר: Number	148463
תאריך: Date	
הוקדם/נדחה: Ante/Post-dated	03 -03- 2002

אני, (שם המבקש, מענו ולגבי גוף מאוגד - מקום התאגדותו)
I, (Name and address of applicant, and in case of body corporate-place of incorporation)

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(באנגלית)
(English)

Pixel sensor array and method of manufacture thereof

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Hereby apply for a patent to be granted to me in respect thereof.

* בקשת חלוקה Application of Division	* בקשת פטנט מוסף Appl. for Patent of Addition	דרישת דין קדימה* Priority Claim		
מבקשת פטנט from application	* לבקשה/לפטנט to Patent/Appl.	מספר/סימן Number/Mark	תאריך Date	מדינת האיגוד Convention Country
No. מס'	No. מס'			
Dated מיום	Dated מיום			

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C. 137841

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חתימת המבקש
Signature of Applicant

For the Applicants,
REINHOLD COHN AND PARTNERS
By : —

This 3 היום of March בחודש 2002 שנת Year

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Pixel sensor array and method of manufacture thereof

Nygon AS

C. 137841

FIELD OF THE INVENTION

This invention relates to pixel sensors for use in cameras, and in particular to such sensors as are used in nuclear and medical imaging systems.

BACKGROUND OF THE INVENTION

Pixel sensors are known to comprise an array of sensor elements such as diodes, and a complementary array of electronics, typically in the form of an ASIC and comprising a charge amplifier and processing electronics for each sensor element. In CCDs such as are used in miniature television cameras and the like, the sensor elements are formed of silicon diodes which are responsive to visible light for producing a current which is amplified by the charge amplifier and subsequently processed.

Pixel sensors for nuclear medical imaging are known that respond to high-energy photons such as X-rays or γ-rays and produce charge in a similar manner. Conventional silicon diodes are not suitable for such applications because they are transparent to the high-energy photons and therefore other materials such as cadmium telluride or mercury iodide are used instead. Since these materials are not based on silicon, the diode cannot be integrated together with the associated electronics as a single monolithic structure and this requires, in practice, that the sensor elements and the associated electronics be manufactured on separate wafers, which are then interconnected using bump bonding.

Fig. 1 shows pictorially a typical arrangement comprising a standalone 2-D pixel sensor depicted generally as 10 and comprising an upper sensor array 11 comprising multiple sensor elements (not shown), each of which is bump-bonded to a corresponding electronics module in a lower ASIC 12. In addition, power and control signals are fed to the sensor 10 and this typically requires that control-pads 13 be formed along at least one edge of the composite chip and which may be connected to external circuitry using wire-bonding 14.

The typical size of each pixel in such an array is 200 μm and the typical dimensions of the two-dimensional array is 1 cm^2. This means that there are typically some 625 pixels per pixel array. In practice, it is usually necessary to image over a much larger area, for example at least 10 x 10 cm^2. This requires that 100 pixel arrays must be packed together, for example as a 10 x 10 matrix. On the one hand, the bump bonding technique used in conventional pixel sensors militates against the closer packing density of the pixels so that it becomes difficult to increase the resolution of the sensor by packing more pixels into a pixel array, since the need to bump-bond each sensor to the corresponding electronics in a different array is a costly process and is subject to low yields. Furthermore, the provision of control-pads along an edge of each module and the need to wire bond these pads to external circuitry means that adjacent sensor arrays cannot be packed edge-to-edge without introducing a "dead" zone where there are, in fact, no pixels at all owing to the interposing I/O and control-pads. Moreover, the connection of the I/O control-pads to the external circuitry by wire bonding is also a costly and cumbersome process and further reduces the effective overall packing density.

EP 0415541 assigned to Shimadzu Corporation, published March 6, 1991 and entitled "*Semiconductor-based radiation image detector and its manufacturing method*" discloses a radiation image detector for detecting a radiation image with the image divided into pixels. The detector comprises a radiation-sensitive semiconductor plate having a common bias electrode deposited on one surface thereof. A plurality of pixel-corresponding signal takeout electrodes are deposited on the other surface of the semiconductor plate, and a plurality of bumps are provided

each of which is fixed on a respective one of the signal takeout electrodes. A passivation film covers each signal takeout electrode where not in contact with its bump, and covering the clearances between the signal takeout electrodes. A base plate is provided with a plurality of contact pads corresponding to and in contact with the bumps.

SUMMARY OF THE INVENTION

It is thus an object of the invention to provide an improved low-cost pixel sensor, which is amenable to closer packing, obviates the above-mentioned drawbacks that are contingent on the use of bump-bonding and the provision of I/O control-pads and allows multiple sensor modules to be juxtaposed so as to form a larger area sensor without requiring any further manufacturing process after assembly.

These objects are realized in accordance with the invention by a method for fabricating a sensor array having a plurality of pixels each including a sensor element coupled to a sensor input of an electronic processing circuit, the method comprising the following steps:

(a) integrating the electronic processing circuits on a wafer so as to form an integrated circuit having at least one array of electronic processing circuits each having a respective sensor input that is accessible from a first surface of the wafer, and

(b) in respect of each pixel, providing an electrically conductive via through the wafer extending from the respective sensor input to a second surface of the wafer opposite the first surface;

thus allowing a respective sensor element to be mounted adjacent the second surface of the wafer and to be electrically connected to the respective electronic processing circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

In order to understand the invention and to see how it may be carried out in practice, a preferred embodiment will now be described, by way of non-limiting example only, with reference to the accompanying drawings, in which:

Fig. 1 shows pictorially a typical prior-art pixel sensor assembly;

Fig. 2 shows pictorially a standard pixel ASIC that is mass-manufactured on a silicon wafer in a first manufacturing step according to the invention;

Fig. 3 shows pictorially the silicon wafer undergoing an optional second manufacturing step according to the invention;

Fig. 4 shows pictorially a third manufacturing step according to the invention;

Fig. 5 shows pictorially a fifth manufacturing step according to the invention for producing ohmic connections between each pixel input and a reverse side of the silicon wafer for allowing direct connection thereto of a pixel sensor;

Fig. 6 shows pictorially the reverse side of the silicon wafer including the multiple ohmic contacts produced according to the invention, each being associated with a respective sensor;

Fig. 7 shows pictorially a sixth manufacturing step according to the invention for depositing sensor material on the reverse side of the silicon wafer;

Fig. 8 shows pictorially a single sensor element according to the invention cut from the wafer shown in Fig. 7;

Figs. 9a and 9b show respectively pictorially top and side elevations of the pixel sensor of Fig. 8 mounted via bump-bonds to a ceramic board in a composite encapsulation having bump-bonds for mounting directly to a PCB motherboard without the need for wire-bonding; and

Fig. 10 shows pictorially a two-dimensional array of encapsulated pixel sensors as shown in Fig. 9 mounted in side-to-side relationship so as to form a composite large array sensor; and

Fig. 11 is a flow diagram summarizing the manufacturing process of a pixel sensor according to the invention.

DETAILED DESCRIPTION OF SPECIFIC EMBODIMENTS

Fig. 2 shows a silicon wafer 20 constituting an integrated circuit or chip, typically formed of a complementary metal oxide semiconductor (CMOS) wafer and being provided with scribe lines 21 so as to form a rectangular matrix of sensor elements 22 each of which, in turn, comprises a matrix of 3 x 5 pixels 23. The wafer 20 is processed at a silicon foundry in known manner and for the purpose of low-cost mass-production is processed according to the invention as an uncut wafer bearing multiple replicas of the same integrated circuit. Each pixel 23 includes a sensor input 24 that is connected to a charge amplifier 25 and a processing unit 26. The charge amplifier 25 together with the processing unit 26 constitute the pixel electronics to which the sensor element (not shown) is connected and which responds to a photon striking the sensor element for measuring the charge produced thereby. Thus, the silicon wafer 20 contains multiple replicas of the pixel array 22 which, after scribing, would produce multiple ASICs each containing an array of 3 x 5 pixel electronic circuits for connecting to a respective sensor element.

Optionally, the standard wafer 20 shown in Fig. 2 may be ground or etched so as to thin down the wafer from the reverse side 28 so as to remove the bulk of the silicon wafer 29, whereby the remainder of the wafer 20 is as thin as practically possible. It is also possible to use a pre-thinned wafer in the IC fabrication described above, in which case subsequent thinning is unnecessary. A pre-thinned wafer will, however, result in a higher manufacturing cost when mass-producing the pixel electronics.

In order to obviate the need for wire bonding as is used in hitherto proposed pixel sensors, the invention connects each sensor input 24 via a respective ohmic contact (or "via") through the silicon wafer to the reverse side thereof. This contact may then be used to connect the sensor element directly to the sensor electronics by effectively bonding the sensor element in correct spatial disposition with respect to the electronics on the reverse side of the silicon wafer. This may be done in various ways, some of which will now be described.

Thus, referring to Fig. 4 the sensor element 24 is coated with extra photomask material 30, which effectively protects the area of the wafer surrounding the sensor input 24, whilst leaving the sensor input 24 itself exposed. It may also be necessary to produce a complementary photomask that covers the same region but is provided on the reverse side 28 of the silicon wafer in precise registration with the photomask that is disposed on the pixel 23. Once this is done, a connection may be formed to the sensor input 24 through the wafer by implanting the silicon wafer with an n-type donor impurity, being a pentavalent material such as antimony, phosphorus or arsenic to which the photomask 30 is impervious, so that the donor impurity penetrates only the sensor input 24 and creates a local increase in the conductivity of the silicon from the sensor input 24 through the wafer 20 to its reverse side, thus effectively forming a matrix of conductive vias 31, each of which connects a respective sensor input 24 to the reverse side of the wafer 20 as shown pictorially in Fig. 6.

An alternative approach is to provide a photomask on the reverse side only of the wafer that exposes the silicon in direct registration with the sensor input on the topside of the wafer and partially to etch holes through the wafer from the reverse side to the sensor input 24, whilst not etching all the way through the wafer. The resulting bores are then filled with conductive material such as aluminum.

Yet another possibility is to combine the two above-mentioned approaches whereby holes are partially etched through the wafer from the reverse side and a p-type impurity, such as boron, is implanted from the top side so as to render the wafer directly underneath each sensor input conductive. The partial bores are then filled with conductive material such as aluminum, which abuts the now-conductive wafer and completes the ohmic contact to the reverse side of the wafer.

Referring to Fig. 7 there is shown a subsequent stage in the manufacturing process where desired amorphous or polycrystalline sensor material such as mercury iodide is grown on the top side of the wafer so as to form an array of diodes, each having an anode which is in ohmic contact with a respect one of the conductive vias 31 (shown in Fig. 6) and such that the opposite surface of the

sensor material forms a common cathode towards which incident photons are directed. Thus, Fig. 7 shows pictorially a composite wafer 35 having a lower silicon wafer 36 as described above, on top of which is grown an amorphous or polycrystalline sensor material 37 so as to form a matrix of sensor elements having a common cathode constituted by the upper surface of the device and a respective anode (not shown) that is effectively sandwiched between the upper sensor layer 37 and the lower silicon wafer 36 and is connected via a corresponding one of the vias formed in the silicon wafer 36.

As shown in Fig. 8, the wafer 35 is now scribed along the scribe lines so as to produce individual sensor chips 40, which in the specific example shown in the figure comprises 5 x 3 pixel elements in a two-layer structure having an upper layer 41 formed of a silicon wafer and having integrated therewith pixel electronics reference 23 in Fig. 4 and having a lower layer 42 on which the sensor elements themselves are deposited. The upper layer 41 also includes I/O and control-pads 43 which are metallized on the outer surface of the silicon wafer in known manner and formed already in an earlier stage of the fabrication corresponding to the silicon wafer 20 shown in Fig. 2. As explained above, pixel sensors are deposited on the lower layer 42, whose outer surface constitutes a common cathode such that the anodes of each sensor element are connected to a corresponding sensor input of the pixel electronics via a corresponding through-connect or via formed through the body of the silicon wafer 41. Likewise, the I/O and control-pads 43 are formed on the outer surface of the silicon layer 41 rather than being brought to edge connections as is typically done in hitherto-proposed configurations. This greatly facilitates mounting of the pixel array and allows multiple pixel arrays to be cascaded in edge-to-edge relationship, resulting in a much more compact configuration with greatly reduced dead space compared to hitherto-proposed configurations.

Figs. 9a and 9b show how the pixel sensor module 40 shown in Fig. 8 may be encapsulated so that the common cathode of the pixel sensor layer 42 is uppermost and the I/O and control pads 43 are connected via bump-bonds 45 to a

ceramic board 46 which are low density and easy to manufacture. The ceramic board 46 feeds bump-connections 47 through to surface mounted pins or bores (e.g., PGA or BGA standard). The complete arrangement is encapsulated so as to form a module 48 that is easily mounted on to a PCB motherboard. The module 48 is very easy to handle and can be mounted as one of many identical elements that are mounted edge-to-edge so as to form a two-sensor having a much larger surface area and minimum dead space as shown pictorially in Fig. 10 where a large sensor array 50 is formed by mounting multiple sensor modules 48 in edge-to-edge arrangement, all surface mounted to a standard PCB assuming that BGA encapsulation is employed. If, alternatively, PGA encapsulation were employed, then the modules 48 would typically be mounted in IC sockets.

It will be apparent that modifications may be made to the assembly without departing from the scope of the invention as claimed which resides, principally, in the provision of ohmic connections that are formed in the silicon wafer so as to allow ohmic connection therethrough of a pixel sensor element to the input connection of the corresponding pixel electronics that is integrated into the silicon wafer on the top side thereof. By such means, the need to interconnect each sensor element to the corresponding electronics in the silicon wafer via bump-connections is avoided thus allowing a much more compact assembly to be produced. Furthermore, since the I/O and controls pads may easily be mounted on the top surface of the silicon, this obviates the need to provide connections along the edge of the pixel assembly, thus rendering the assembly still more compact and allowing easy expansion of the pixel array by mounting multiple modules edge-to-edge with minimum intervening dead space.

Fig. 11 is a flow diagram summarizing the essential features of the above-described manufacturing process of a pixel sensor according to the invention.

Whilst, in the preferred embodiment as described above, the sensor elements are themselves deposited using mercury iodide on to the silicon wafer, it will be appreciated that other materials may be used such as cadmium zinc telluride and cadmium mercury iodide. Likewise, the invention contemplates the sensor elements

being provided as a completely separate integrated unit, whose multiple sensor elements may each be connected to a respective pixel electronics unit in the silicon layer via the ohmic contact formed therethrough according to the invention. Thus the invention also contemplates the situation where the sensor elements and the sensor electronics are formed in discrete layers, which are bonded together rather than being formed as a monolithic structure.

Furthermore, while a preferred embodiment has been described with regard to CMOS circuitry, it will be appreciated that the principles of the invention are applicable to other technologies.

Although use of such sensors in nuclear and medical imaging systems has been mentioned, it is to be noted that the invention is not limited to any particular application. Thus, other applications of the invention will be apparent to one skilled in the art and include, without limitation, X-ray computed tomography; night vision sensors; standard medical and industrial X-ray devices; nuclear medicine PET/SPECT sensors; particle detectors; X-ray diffraction detectors and others.

It should also be noted that in the fabrication stage shown in Fig. 8, the wafer does not need to be divided along every scribe line. Thus, in the example described in the preferred embodiment where each pixel sensor comprises an array of 3 x 5 pixels, a larger array of 6 x 5 pixels can be fabricated simply by not scribing between two adjacent pixel arrays. Likewise, an array of 6 x 10 pixels can be formed by suitable division of the wafer 20. In saying this, it is of course to be noted that the invention is not limited to any specific number or arrangement of pixels in each pixel array and the usual cost/yield considerations apply. Thus, by reducing the number of pixels in each array, fewer pixels are wasted upon discarding faulty pixel arrays. Theoretically, one large pixel array could be formed using the complete area of the wafer; but in this case a fault in a single pixel would require that the complete wafer be discarded.

In the preferred embodiment, the electronic processing circuits include amplifiers and further processing circuitry. This allows incident photons to trickle charge the pixel array and to be counted on impact. However, this also is not

intended to limit the invention since at their most basic the electronic processing circuits can be simply capacitors that store the incoming charge, in a manner somewhat analogous to a CCD, where charge is read out sequentially similar to a shift register.

In the method claims that follow, alphabetic characters and Roman numerals used to designate claim steps are provided for convenience only and do not imply any particular order of performing the steps.

CLAIMS:

1. A method for fabricating a sensor array having a plurality of pixels each including a sensor element coupled to a sensor input of an electronic processing circuit, the method comprising the following steps:

(a) integrating the electronic processing circuits on a wafer so as to form an integrated circuit having at least one array of electronic processing circuits each having a respective sensor input that is accessible from a first surface of the wafer, and

(b) in respect of each pixel, providing an electrically conductive via through the wafer extending from the respective sensor input to a second surface of the wafer opposite the first surface;

thus allowing a respective sensor element to be mounted adjacent the second surface of the wafer and to be electrically connected to the respective electronic processing circuit.

2. The method according to Claim 1, further including:

(c) growing the sensor elements on the second surface of the integrated circuit, each in registration with a corresponding one of the sensor inputs.

3. The method according to Claim 1 or 2, wherein the integrated circuit includes multiple arrays of pixels and there is further included the step of:

(d) dividing the integrated circuit into discrete sensor arrays.

4. The method according to any one of Claims 1 to 3, further including:

(e) assembling multiple sensor arrays edge to edge so as to form a composite sensor array having an extended surface area.

5. The method according to any one of Claims 1 to 4, further including:

(f) thinning down the wafer from a reverse side thereof so as to remove the bulk of the wafer.

6. The method according to any one of Claims 1 to 4, wherein the wafer is pre-thinned prior to carrying out step **(b)**.

7. The method according to any one of Claims 1 to 6, wherein step **(b)** includes:

i) coating a top side of the wafer with photomask for protecting an area surrounding the sensor input, whilst leaving the sensor input exposed, and

ii) implanting the wafer with a material to which the photomask is impervious, so that said material penetrates only the sensor input and creates a local increase in the conductivity of the wafer from the sensor input through the wafer to a reverse side thereof, thus forming a matrix of conductive vias, each of which connects a respective sensor input to the reverse side of the wafer.

8. The method according to Claim 7, further including:

iii) producing a complementary photomask that covers said area of the wafer on the reverse side thereof and is in precise registration with the photomask that is disposed on the top side thereof.

9. The method according to Claim 7 or 8, wherein the wafer is based on silicon and said material is a p-type impurity.

10. The method according to any one of Claims 1 to 6, wherein step **(b)** includes:

i) providing a photomask on the reverse side only of the wafer so as to exposes the wafer in direct registration with the sensor input on the top side of the wafer,

ii) etching holes through the wafer from the reverse side to the sensor input, whilst not etching all the way through the wafer so as to form bores, and

iii) filling the bores with conductive material.

11. The method according to any one of Claims 1 to 6, wherein step **(b)** includes:

i) partially etching holes through the wafer from the reverse side so as to form partial bores,

ii) implanting the wafer from the top side thereof with a material to which the photomask is impervious, so that said material penetrates only the sensor input and renders the wafer directly underneath each sensor input conductive, and

iii) filling the partial bores with conductive material which abuts the wafer and completes the ohmic contact to the reverse side of the wafer.

12. The method according to any one of Claims 1 to 11, further including:

(g) growing amorphous or polycrystalline sensor material on the top side of the wafer so as to form an array of diodes, each having an anode which is in ohmic contact with a respect one of the conductive vias and such that an opposite surface of the sensor material forms a common cathode.

13. The method according to any one of Claims 1 to 12, wherein the integrated circuit includes multiple arrays of electronic processing circuits separated by scribe lines and there is further included:

(h) scribing along the scribe lines so as to produce individual sensor chips.

14. The method according to any one of Claims 1 to 13, further including:

(i) connecting I/O and control pads metallized on an outer surface of the wafer via bump-bonds to a ceramic board that feeds bump-connections through to surface mounted pins or bores, and

(j) encapsulating so as to form a module.

15. The method according to Claim 14, further including:

(k) mounting several of said modules edge to edge so as to form a two-dimensional sensor of larger surface area than a single module.

16. A sensor array or module manufactured according to any one of Claims 1 to 15.

For the Applicants,
REINHOLD COHN AND PARTNERS
By:

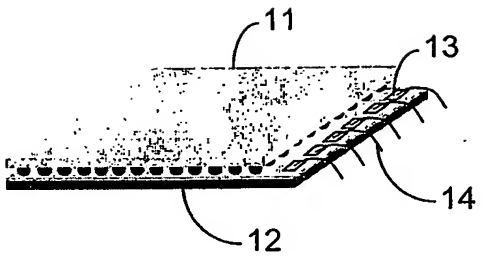

FIG. 1

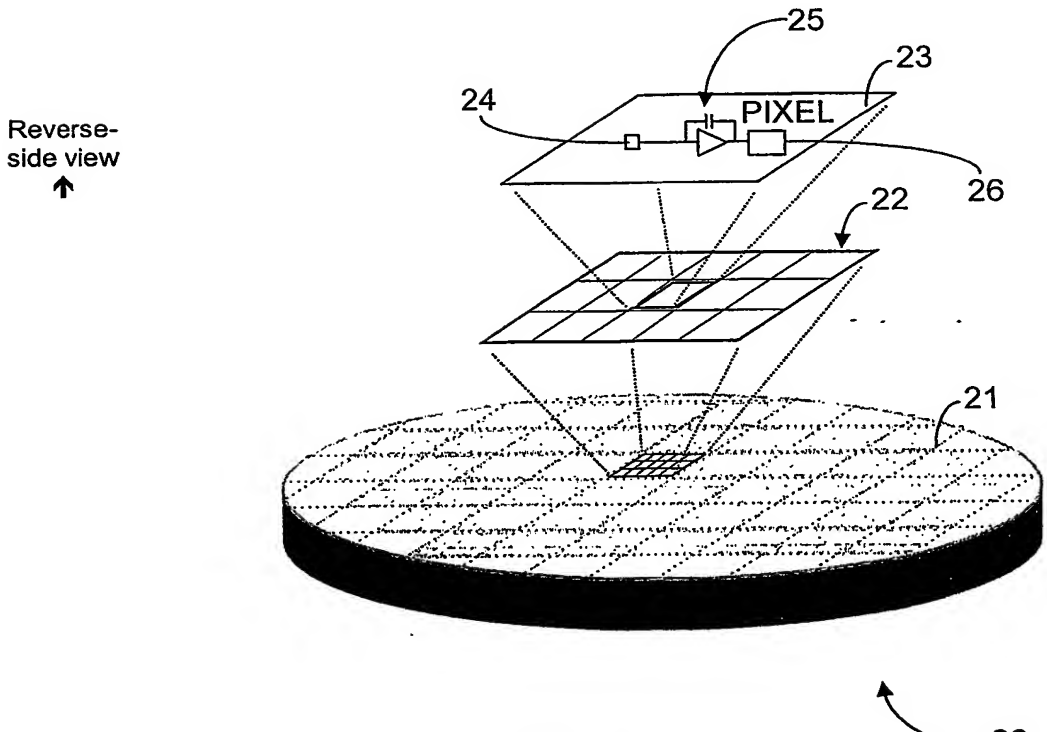

FIG. 2

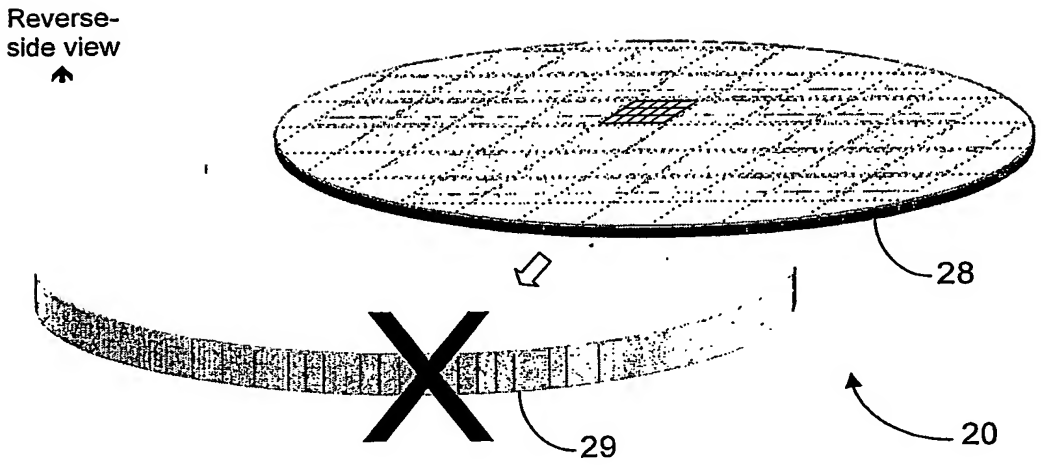
Reverse-
side view
28
29
20

FIG. 3

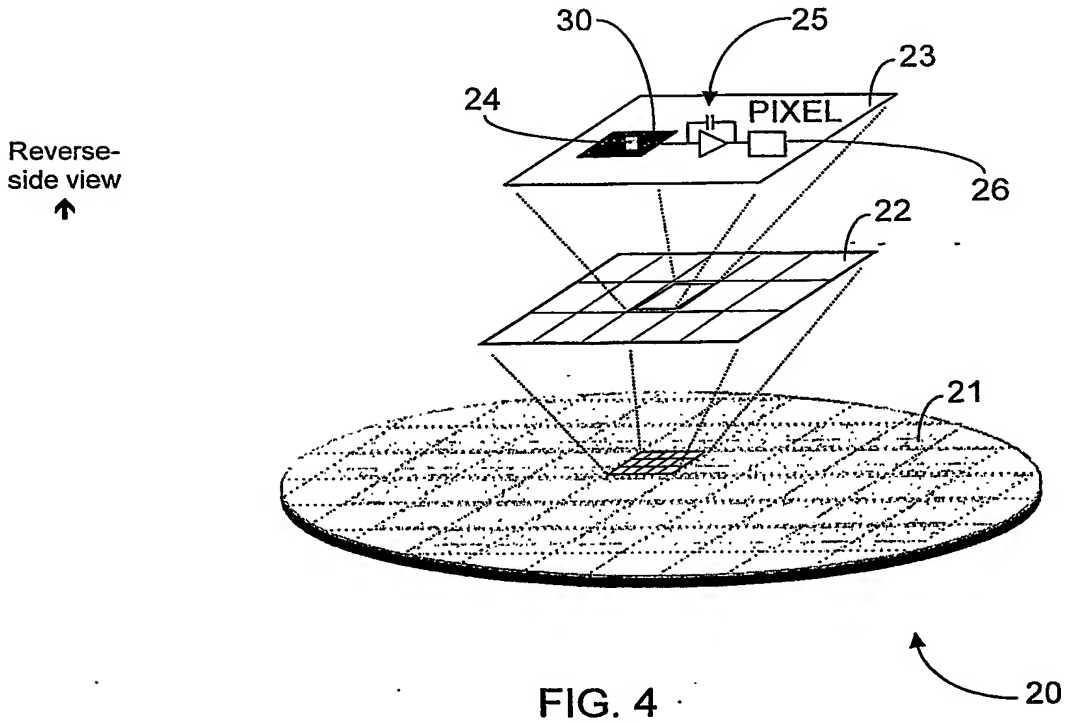
Reverse-
side view
30
25
23
24
PIXEL
26
22
21
20

FIG. 4

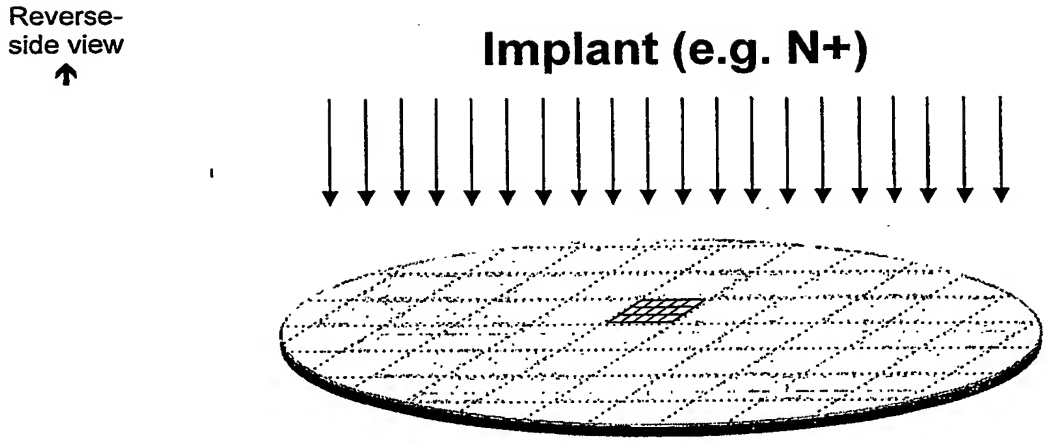
Reverse-side view
Implant (e.g. N+)

FIG. 5

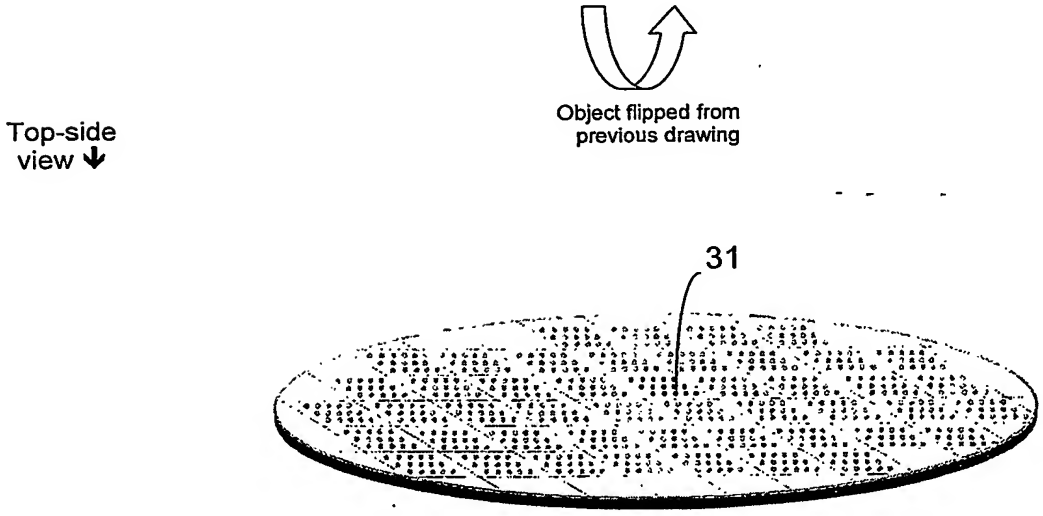
Object flipped from previous drawing
Top-side view
31

FIG. 6

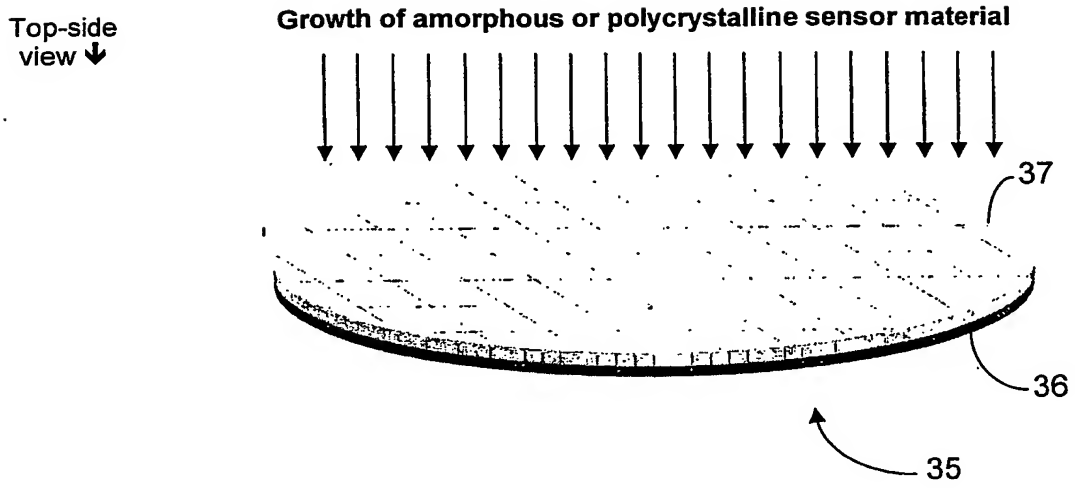
Top-side view
Growth of amorphous or polycrystalline sensor material
37
36
35

FIG. 7

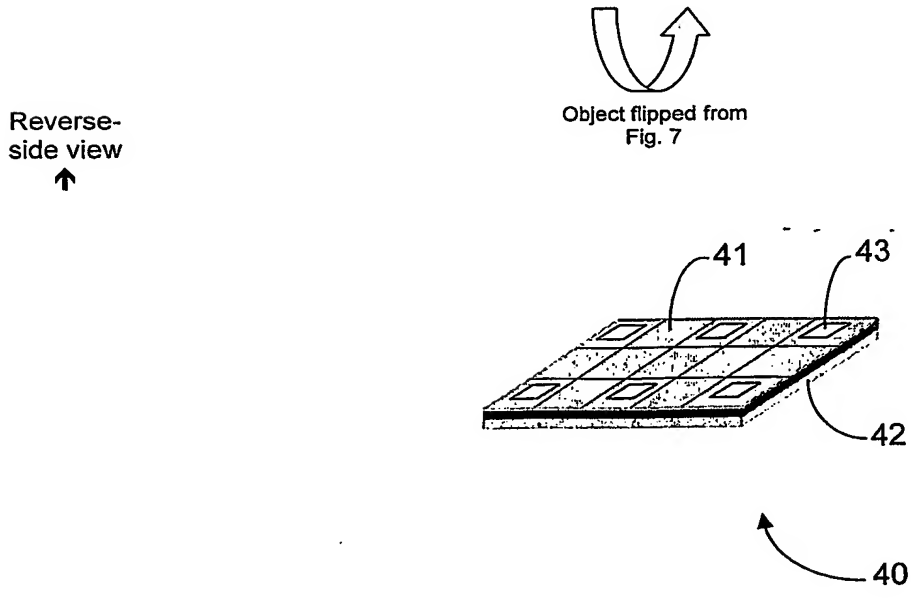
Object flipped from Fig. 7
Reverse-side view
41
43
42
40

FIG. 8

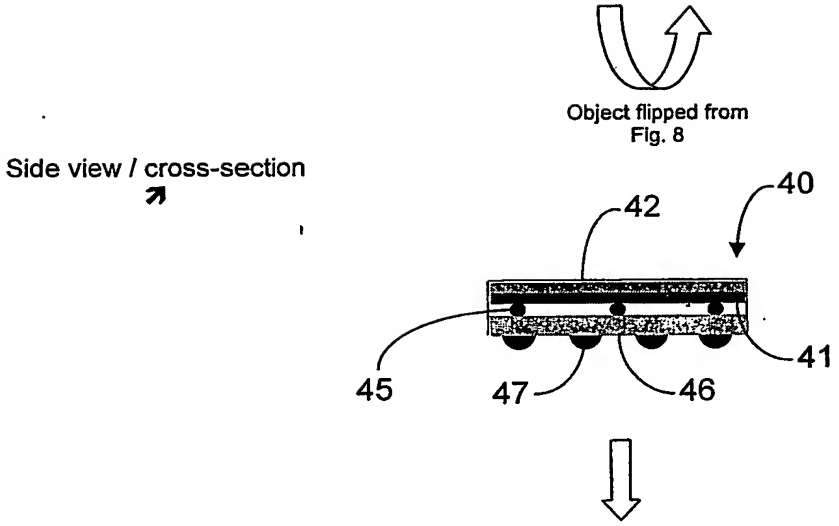

FIG. 9a

FIG. 9b

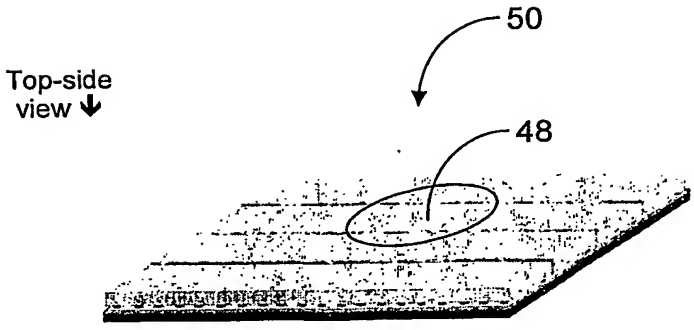

FIG. 10

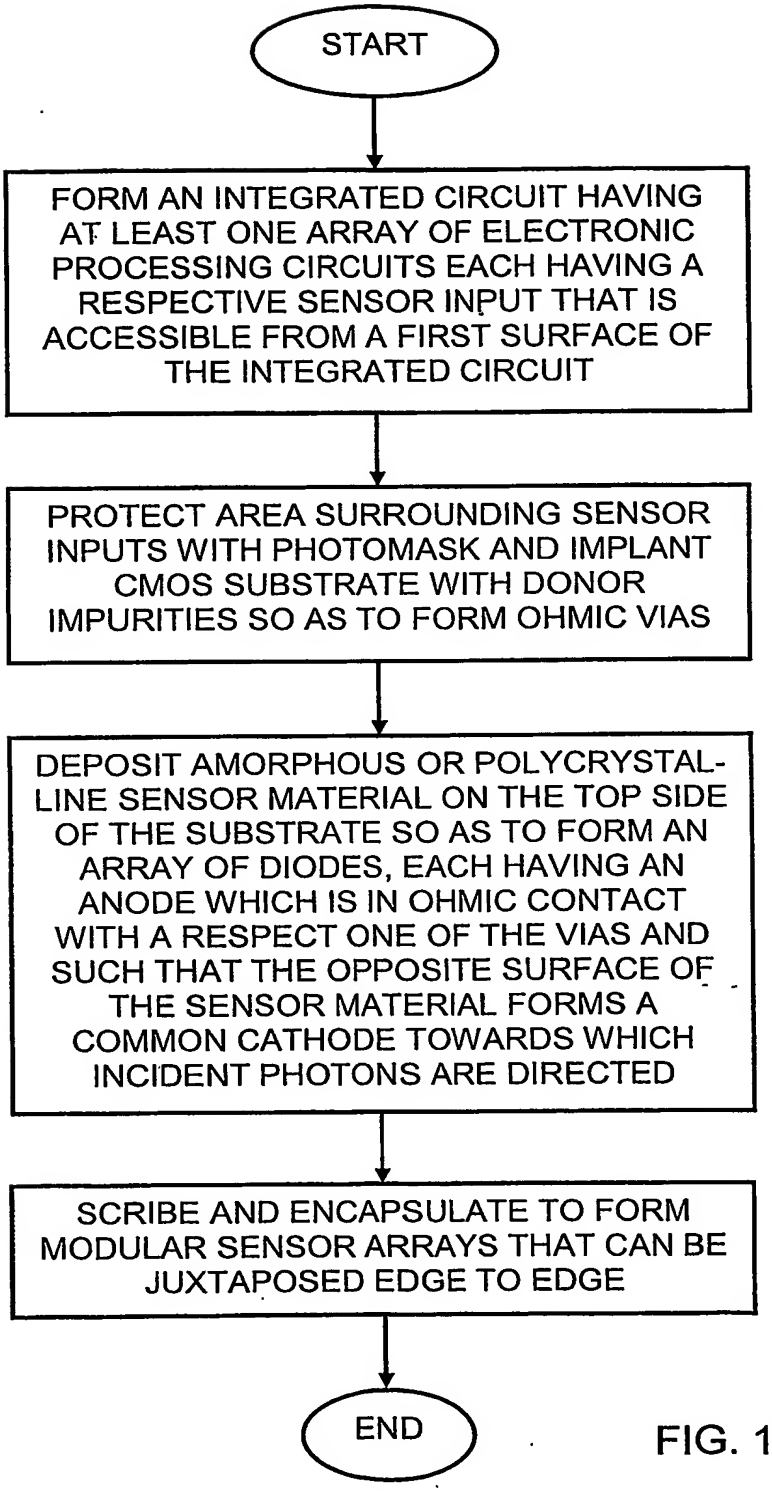
START
FORM AN INTEGRATED CIRCUIT HAVING AT LEAST ONE ARRAY OF ELECTRONIC PROCESSING CIRCUITS EACH HAVING A RESPECTIVE SENSOR INPUT THAT IS ACCESSIBLE FROM A FIRST SURFACE OF THE INTEGRATED CIRCUIT
PROTECT AREA SURROUNDING SENSOR INPUTS WITH PHOTOMASK AND IMPLANT CMOS SUBSTRATE WITH DONOR IMPURITIES SO AS TO FORM OHMIC VIAS
DEPOSIT AMORPHOUS OR POLYCRYSTAL-LINE SENSOR MATERIAL ON THE TOP SIDE OF THE SUBSTRATE SO AS TO FORM AN ARRAY OF DIODES, EACH HAVING AN ANODE WHICH IS IN OHMIC CONTACT WITH A RESPECT ONE OF THE VIAS AND SUCH THAT THE OPPOSITE SURFACE OF THE SENSOR MATERIAL FORMS A COMMON CATHODE TOWARDS WHICH INCIDENT PHOTONS ARE DIRECTED
SCRIBE AND ENCAPSULATE TO FORM MODULAR SENSOR ARRAYS THAT CAN BE JUXTAPOSED EDGE TO EDGE
END

FIG. 11